

**DISTRIBUTED TIME-MULTIPLEXED BUS ARCHITECTURE  
AND EMULATION APPARATUS**

**ABSTRACT OF THE DISCLOSURE**

5           A time-multiplexed data bus driver circuit includes a plurality of combinatorial  
circuits, each of the circuits forming a logic combination of a datum value, a datum  
enable signal and a datum timeslot signal, the plurality of circuits producing a plurality  
of output signals based thereon, and a wired-OR junction producing a logic OR  
combination of the plurality of output signals representing a time-multiplexed data  
10 stream. Preferably, for each of the combinatorial circuits the enable signal, the timeslot  
signal and the datum signal (and preferably also a clock signal) are combined in an  
AND function to produce a gating signal for an active-low datum value, one selected  
active-low datum value being gated onto the wired-OR junction at a given timeslot  
when enabled. The common time-multiplexed data channel at the wired-OR junction  
15 has a pre-charge circuit for biasing the junction to a positive or ground voltage, thereby  
representing in an un-driven state a respective logic 1 or 0.